REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the following discussion is respectfully requested.

Claims 1-20 remain active in this case.

In the outstanding Office Action, Claims 1, 2 and 7-13 were rejected under 35 USC 103(a) as unpatentable over Kim et al (US 5,929,691, hereinafter called "Kim '691") in view of Kim et al (US 6,150,868, hereinafter called "Kim '868") and further in view of Verwegen (US 6,147,546); Clam 3 rejected under 35 USC 103(a) as unpatentable over Kim '691 in view of Kim '868" in view of Verwegen, and further in view of Saito et al (US 6,320,800, hereinafter called "Saito"); and Claims 4-6 and 14-17 were rejected under 35 USC 103(a) as unpatentable over Kim '691 in view of Kim '868 in view of Verwegen, and further in view of Saito and Kang (US 6,134,177)..

Applicants respectfully traverse the outstanding grounds for rejection, because in Applicants view, the grounds for rejection are based on a misreading of the teachings of the references and in fact the pending claims clearly patentably define over the cited prior art.

In particular, with respect to Kim '691, it is respectfully submitted that the outstanding Official Action has overlooked a significant difference between the invention of Kim '691 and the claimed invention. The position of the fuse disclosed by FIG. 7 of Kim '691 and the position of the fuse disclosed by FIG. 6 (corresponding to Claim 1) of the present application are different. In other words, in FIG. 7 of Kim '691, fuse 31 is arranged outside two MOS FETs 23 and 24 (i.e. on the side of a power supply terminal), which configure an inverter. On the other hand, in FIG. 6 of the present application, the fuse is arranged inside two MOS FETs P1A and N1A (i.e. on the side of an output node), which configure and inverter. The outstanding Office Action does not recognize this difference.

However, the claimed invention by virtue of this difference achieves advantages (1)-(5), described below, which cannot be achieved by Kim '691. Further, none of Kim '868, Verwegen, Saito, Kang or Potter et al. (US 6,308,230) of record discloses the above-described structure of the claimed invention. Therefore, it is respectfully submitted that the claimed invention is not obvious over these references.

Practical advantages of the claimed invention over the cited prior art are next described in the following several examples (1)-(5).

(1) If fuse 31 were cut in the circuit shown in FIG. 7 of Kim '691, and if a load capacitance were applied to the source of MOS FET 34, the potential of node N33 would become unstable, and the circuit may malfunction, but this will not occur in the circuit of the claimed invention.

(2) If fuse 31 were cut in the circuit shown in FIG. 7 of Kim '691, inverter 35 may malfunction by being affected by MOS FET 34, but this will not occur in the circuit of the claimed invention.

(3) With the circuit shown in FIG. 7 of Kim '691, a let-through current may flow through due to a malfunction as described above under (1), but with the claimed invention, a let-through current would not flow through the circuit.

(4) With the structure shown in FIG. 7 of Kim '691, an output terminal of inverter 35 would be affected by an external wiring capacitance. However, inverter INV2 is provided in the circuit shown in FIG. 6 of Applicants' disclosure, and therefore, an output terminal of inverter INV1A will not be affected by an external wiring capacitance.

(5) With the claimed invention, even if the initialization pulse width of a fuse latch circuit were small, the circuit would operate stably and at a high speed.

Turning now to the Verwegen reference, the circuit structure disclosed in FIG. 3 of Verwegen would cause a let-through current to flow. When INIT = "H", an output signal of NOR 8 would be "L", and an output signal of inverter 1 would be "H". As a result, an output signal of inverter 3 would be "L". In such a case, an output signal of OR 9 would be "H", and MOS FET 7 would be turned ON. Since MOS FET 6, which configures the inverter 1, is turned ON, a let-through current would flow from Vdd to Vss, by way of MOS FETs 6 and 7. Accordingly, when INTI = "H", a let-through current would flow through the circuit, thereby increasing the consumption of power. In addition, the layout of the circuit of FIG. 3 is complex, and the structure requires a large number of elements.

With respect to Kim '868, the circuit structure disclosed by this reference has the same problem as the circuit structure of Verwegen, which is that a let-through current flows in the circuit, and that the layout of the circuit is complex.

With respect to Saito, Saito relates to redundancy technology, which is different from the problem addressed by the claimed invention.

Similarly, the circuit structure taught by Kang is different from that of the claimed invention.

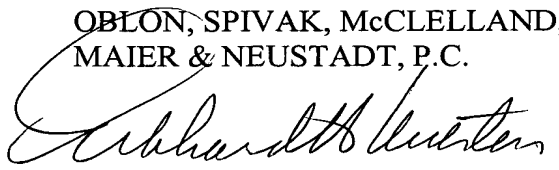
The invention disclosed by Potter et al. relates to a communication interface for an embedded microcomputer device controller, which is different from the claimed invention.

Accordingly, in view of the above comments, it is respectfully submitted that the outstanding grounds for rejection have been traversed. No further issues are believed to be

outstanding, and the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

I:\ATTY\EHK\24's\248965\248965US-REQUEST FOR RECONSIDERATION-4.12.06.DOC